



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

In Re: Fang Xu

Serial No: 10/675,083

Filed: September 30, 2003

For: EFFICIENT SWITCHING
ARCHITECTURE WITH
REDUCED STUB LENGTHS

Group: 2829

Examiner: Patel, Paresh

April 26, 2005

CERTIFICATE OF MAILING, EXPRESS MAIL, OR TRANSMISSION

I, DoNique Hill, certify that—

☒ this correspondence was placed in an envelope addressed to Commissioner for Patents, P.O. Box 83, Alexandria, VA 22313-1450, and I have a reasonable basis to believe that it will be deposited with the US Postal Service as first class mail, postage prepaid, to the U.S. Patent and Trademark Office on December 22, 2004

Signature: _____

Date: April 26, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir or Madam:

In accordance with the duty of candor, this statement is being filed before the mailing date of any of a final action under § 1.113, a notice of allowance under § 1.311, an action that otherwise closes prosecution in the application, or on or before payment of the issue fee, and it is accompanied by a statement specified in 37 C.F.R. 1.97 (e):

Each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement.

This information disclosure statement is not to be construed as a representation that a search has been made, nor is it to be construed as an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in § 1.56(b).

No fee is believed to be due; however, if any fees are due please apply such fees to Deposit Account Number 20-0515 referring to Attorney Docket Number 1765-US.

Respectfully Submitted,

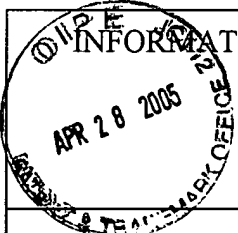


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 INFORMATION DISCLOSURE STATEMENT				Atty. Docket No. 1766-US		Serial No. 10/675,083		
				Applicant: Fang Xu				
				Filing Date: 9/30/2003		Group: 2829		
U.S. PATENT DOCUMENTS								
Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if appropriate	
	AA	2003/0043015	3/6/2003	Gershfeld	340	2.28	8/28/2001	
	AB	4,798,435	1/17/1989	Fujiwara et al.	350	96.13	5/16/1985	
	AC							
	AD							
	AE							
	AF							
FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AG	56117495	9/14/1981	Japan	3/64	17/00		X
	AH	2 538 912 A	7/6/1984	France				X
	AI							
OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)								
	AJ	International Search Report						
	AK	"LOGICALLY CONTROLLED CHIP INTERCONNECTION TECHNIQUE" IBM Technical Disclosure Bulletin, IBM Corp. New York, US - vol. 32, no 3B, 1 August 1989 (1989-08-01), pages 294-299, XP000029849, ISSN: 0018-8689, figure 3						
	AL	PATENT ABSTRACT OF JAPAN, JP 56 117495 A (Meisei Electric Co Ltd), 14 September 1981 (1981-09-14) abstract; figures 1,3						
	AM							
	AN							
	AO							
Examiner				Date Considered				
Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.								